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# Impedance plane analysis of class DE amplifier

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*Indexing terms: Power amplifiers, Circuit design*

The class DE RF power amplifier is analysed in the normalised effective load impedance plane. The conditions for zero voltage switching (ZVS) and class E switching transitions are obtained. A proposed matching network allows ZVS operation for any resistive load. Class DE transistor utilisation approaches that of class D.

*Introduction:* Class D and E switching RF power amplifiers are theoretically 100% efficient. In practice class D suffers from switching loss, while class E employs zero voltage switching (ZVS) to reduce it; class E also has $dv/dt = 0$ which gives low parameter sensitivity. However, the single-ended class E circuit [1,2] imposes a much higher voltage stress on the switches than the push-pull class D. A hybrid combining the best of both circuits was first proposed by Zhukov and Kozyrev [3] in 1975, but this work was unknown in the West. Steigerwald [4] noted the use of ZVS in a class D circuit, but did not analyse it. Recently the class DE circuit was rediscovered by Koizumi *et al.* [5,6] (who employed a duty factor of 25%), and independently by El-Hamamsay [7]. In this Letter the generalised class DE amplifier is analysed.

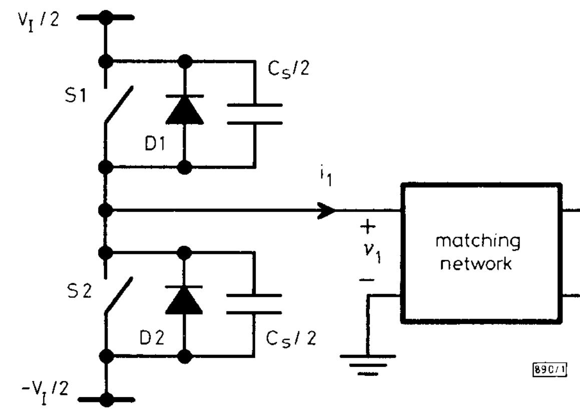


**Fig. 1** *Generalised class DE amplifier*

*Analysis:* Fig. 1 shows the circuit, and Fig. 2 its waveforms. For convenience the DC input is $\pm V_I/2$. An ideal switch, a diode and a capacitance of $C_s/2$, model a switching device such as a MOSFET. A high $Q$ matching network forces the inverter's output current waveform $i_1(t)$ to be almost sinusoidal, so let $i_1(t) = I_{1pk}\sin(\omega t - \phi)$, where $\omega$ is the angular switching frequency and $\phi \in [0, \pi]$. When $S2$ opens at $t = 0$, the total switch capacitance $C_s$ is charged by the negative $i_1$, raising the inverter's output voltage $v_1$from $-V_I/2$ until it reaches $V_I/2$ at $t = t_0$. $D1$ prevents $v_1$ from rising further, so $S1$ can be turned on with ZVS at $t \geq t_0$. The other half cycle is similar.

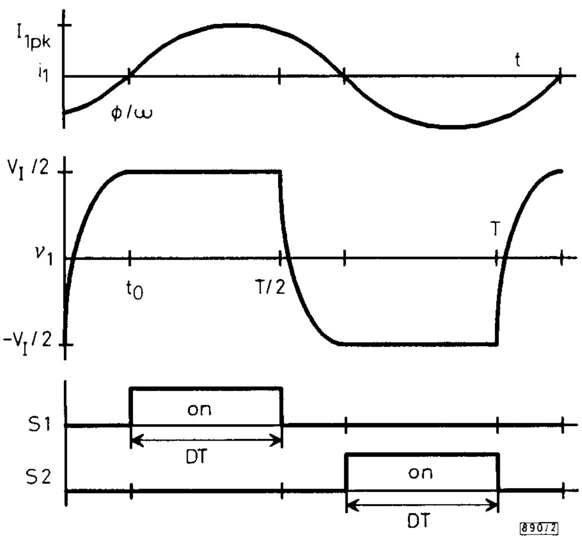


**Fig. 2** *Class DE waveforms*

For class E transitions, $dv_1/dt = 0$ at $t_0$. Therefore $i_1(t_0) = 0$, giving $\phi = \omega t_0$. If each switch operates with a duty factor $D \in [0, 0.5]$, then from Fig. 2, $D = (\pi-\phi)/2\pi$. To swing $v_1$ from $-V_I/2$ to $V_I/2$, capacitance $C_s$ must be supplied with charge $C_s V_I = \int i_1(t)dt$. Integrating and solving for $I_{1pk}$,

$$I_{1pk} = \frac{\omega C_s V_I}{1 - \cos\phi} \qquad (1)$$

(Note that a small phase angle $\phi$ implies a large peak current.) Substituting for $i_1$ in $dv_1/dt = -i_1/C_s$ and integrating,

$$v_1(t) = V_I \frac{2\cos(\omega t - \phi) - (1 + \cos\phi)}{2(1 - \cos\phi)} \quad t \in [0, t_0] \qquad (2)$$

The normalised effective load impedance plane (NELIP) technique is now employed. Current $i_1(t)$ is represented by phasor $\mathbf{I}_1$, and the fundamental component of $v_1(t)$ by phasor $\mathbf{V}_1$. (The high $Q$ matching network rejects the harmonics.) By Fourier analysis,

$$\mathbf{V}_1 = \frac{4}{T}\left(\int_0^{t_0} v_1(t)\exp(-j\omega t)dt + \int_{t_0}^{T/2} \frac{V_I}{2}\exp(-j\omega t)dt\right)$$
$$= V_I \frac{\phi\cos\phi - \sin\phi - j\phi\sin\phi}{\pi(1 - \cos\phi)} \qquad (3)$$

and

$$\mathbf{I}_1 = \frac{2}{T}\int_0^T I_{1pk}\sin(\omega t - \phi)\exp(-j\omega t)dt$$
$$= -\frac{\omega C_s V_I(\sin\phi + j\cos\phi)}{1 - \cos\phi} \qquad (4)$$

The effective impedance seen by the inverter is $\mathbf{Z}_1 = \mathbf{V}_1/\mathbf{I}_1 = R_1 + jX_1$, say. Normalising $R_1$ and $X_1$ by multiplying by $\omega C_s$ [2] yields the dimensionless quantities

$$R_1' = \frac{1 - \cos 2\phi}{2\pi} \quad \text{and} \quad X_1' = \frac{2\phi - \sin 2\phi}{2\pi} \qquad (5)$$

The NELIP (Fig. 3) is the $R'_1 - X'_1$ plane, and eqn. 5 describes parametrically the locus of class DE operation. (The locus is a cycloid, the curve traced out by a point on the circumference of a circle of radius $1/2\pi$ as it rolls on the $X'_1$ axis.) Values of $D$ are also marked. Class DE waveforms have been verified by PSPICE simulation at various points on the locus.

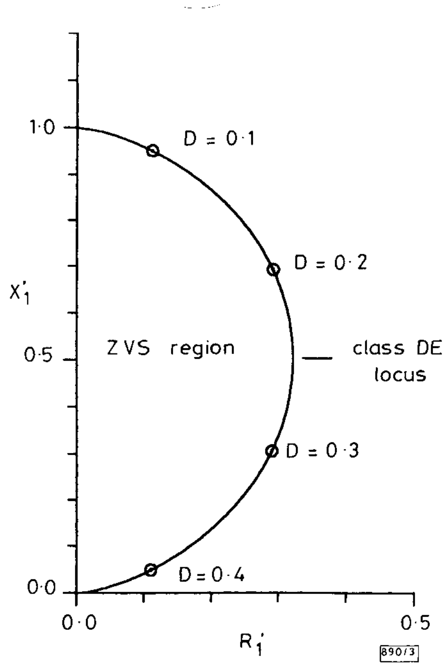


**Fig. 3** *Complex $Z'_1$ plane (NELIP), showing locus of class DE operation and ZVS region*

$I_{1pk}$ is increased beyond the value given by eqn. 1, the transitions change from class E to ordinary ZVS, in the region lying between the class E locus and the $X'_1$ axis. Outside this region $v_1$ does not reach $V_I/2$. Further analysis is beyond the scope of this Letter.

*Choice of matching network:* The design of the matching network is straightforward for a fixed load, but with a variable load resistance $R$, each value of $R$ maps to a point in the NELIP. For efficient operation the resulting locus should remain within the ZVS region. The matching network may be designed to map $R = 0$ and $R = \infty$ to the $X'_1$ axis between 0 and 1, protecting the transistors against abnormal loads. The matching network of Fig. 4 can achieve this.

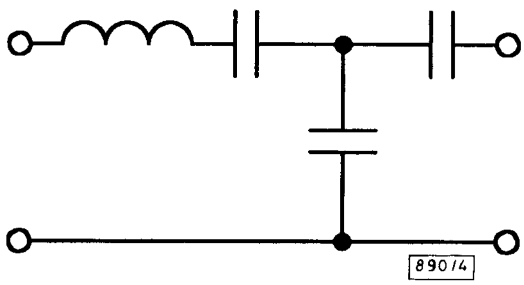


**Fig. 4** *Proposed matching network*

*Switch utilisation:* A utilisation factor for the switches in an ideal power converter may be defined by $U = P/(V_{max} I_{max} n)$, where $P$ is the power throughput, and $V_{max}$ and $I_{max}$ are the voltage and current stresses on each of the $n$ switches. $U$, which lies between 0 and 1, is useful for comparing diverse topologies. For class DE,

$$P = \frac{1}{2}\mathrm{Re}\mathbf{V}_1\mathbf{I}_1^* = \frac{V_I^2 \omega C_s}{2\pi} \cdot \frac{1+\cos\phi}{1-\cos\phi} \qquad (6)$$

Also $V_{max} = V_I$, $I_{max} = I_{1pk}$, given by eqn. 1, and $n = 2$. Hence $U = (1 + \cos\phi)/4\pi$. Its best value, $U = 0.159$, is obtained when $\phi \to 0$ ($D = 0.5$: classical class D). The optimum class E amplifier has $U = 0.098$ [2], which the class DE amplifier attains with $D = 0.29$.

Having low voltage stress, low switching loss and acceptable switch utilisation, the class DE circuit makes an outstanding RF power amplifier. With a suitable rectifier, it should find further application in DC-DC conversion.

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## Influence of lowpass filter on input sensitivity of 1/2 regenerative frequency divider

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*Indexing term: Frequency dividers*

It is found that Miller's classical analysis of 1/2 regenerative frequency dividers produces large errors in cases where low-order loop filters are used. The infeasibility of 1/2 dividers with first-order lowpass filters is demonstrated. An accurate analytical expression is proposed for the input sensitivity of a 1/2 divider with a second- and a third-order lowpass filter, based on the application of the harmonic balance technique.

*Introduction:* The principle of regenerative frequency division described by Miller [1] has recently been applied in integrated circuits for realising high-frequency low-power dividers [2–4]. Although the performance of a 1/2 regenerative frequency divider (RFD) is largely dependent on the ability of the lowpass filter to suppress the odd harmonics $3\omega_{in}/2$, $5\omega_{in}/2$, ... that inherently appear in the loop ($\omega_{in}$ is the input angular frequency), no attempt has yet been made to take these harmonics into account, and the simplifying assumptions of [1] have been widely adopted regardless of the filter performance. Thus, from Fig. 1, if the multiplier's gain is $K$ and the transfer function of the filter is $H(s)$, the input sensitivity of the RFD for a sinusoidal input signal is obtained as [1]

$$A_{min} = \frac{2}{K}\frac{1}{|H(j\omega_{in}/2)|} \qquad (1)$$

It is shown in this Letter that eqn. 1 conceals the fact that frequency division cannot even be achieved with a first-order filter. It is also shown that the application of this formula leads to significant errors in the case of a second-order filter, but the approximation becomes acceptable for filters of order three and higher. An accurate expression is derived for $A_{min}$ and simulation results are given to illustrate its validity.

*Analysis of RFD:* The analysis of the RFD will be performed in three cases, as follows: