

DH Phenomenon in DC/DC Converters

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Abstract-This paper gives analysis of the DH phenomenon in switching power converters caused by the diode reverse recovery, comprising output voltage increase considerably beyond that predicted by the usual analysis and self-sustaining quasiperiodic oscillations. The theoretical results are confirmed by experiment. Design guidelines are presented to avoid overvoltage and instability in practical converters.

I. INTRODUCTION

PWM and resonant switching converters operating at high switching frequencies have complex voltage and current waveforms. This necessitates the use of many approximations in their analysis [1–4]. The most common is the use of ideal switches as models for the semiconductor devices. For resonant converters, to further simplify the analysis and design, the fundamental-component method is frequently used [3, 5]. This gives good results when the loaded Q factor is high and the switching frequency is close to the resonant frequency. However, such an analysis cannot predict all effects, some of which can cause the practical circuit to exhibit unexpected and sometimes strange behaviour.

In this paper we are concerned with the so called DH phenomenon in a high frequency bridge rectifier fed by an inductive source, as shown in Fig.1. This rectifier (or similar) forms part of many switching power converters. The inductance can be introduced intentionally, or it can come from leakage and stray inductances. In particular, it forms an essential part of the series-resonant converter, where this effect was first noticed [6]. Analysing these converters using ideal switches, explicit equations can be obtained for the output voltage V_o . According to these equations, the output voltage is always lower than the input drive voltage [3, 5]. However, in

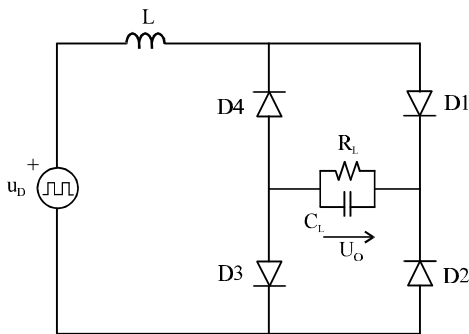


Fig. 1. Class D bridge rectifier fed by inductive drive

practical converters with certain circuit parameters, e.g. when the rectifier circuit employs slow power diodes or has light loading, there are considerable deviations from ideal operation.

These deviations are clearly depicted in Fig. 2, which shows how the measured output voltage depends on the drive frequency. The circuit has the following parameters: $V_{D,pk-pk} = 10V$, $L = 9.42$ mH, four diodes MR752 with storage delay time $t_{sd} = 5$ μs (or recombination lifetime $t = 7.2$ μs), $C_L = 61.5$ nF and load $R_L = 10$ k Ω . At high frequencies, the output voltage rises and at 43 kHz it reaches its maximum: 2.45 times that predicted by analysis, $V_{D,pk-pk}/2$. At frequencies below the maximum, the output voltage oscillates between two levels, depicted by two lines in Fig. 2.

This oscillation were first described in [6] and subsequently named the *DH phenomenon* [8, 9]. Fig. 3 shows the bridge rectifier's input voltage. This square wave voltage appears amplitude-modulated at a frequency apparently unrelated to the switching frequency (quasi-periodicity). The output voltage follows the envelope of the bridge voltage and thus has the same modulation. This might cause the converter to malfunction, especially if it enters a control loop.

The above behaviour is quite robust: it exists for a wide range of circuit parameters and with different diode types [7, 9]. It is found in [6] that this behaviour is caused by the diodes' nonlinear transient characteristics, e.g. reverse recovery. Similar effects occur frequently in practice, but they are rarely

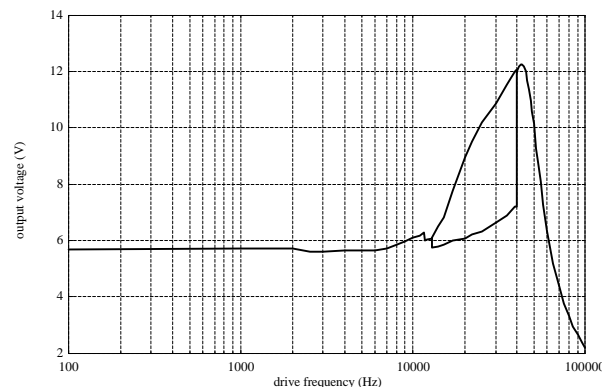


Fig. 2. Measured output voltage dependence on the drive frequency in the circuit of Fig. 1. The output voltage is considerably higher than that predicted by analysis. From 14 kHz to 41 kHz, the output voltage oscillates between two levels.

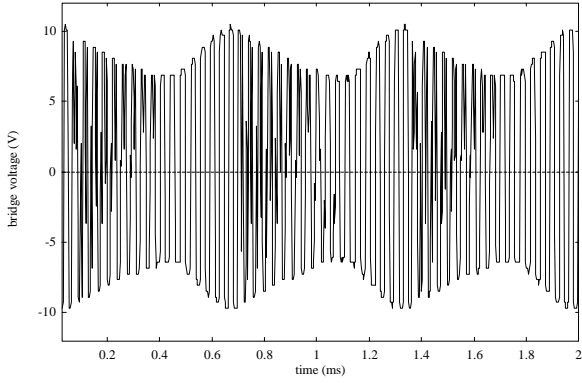


Fig. 3. DH phenomenon in series-resonant converter: Case when $f = 27$ kHz

reported in the literature and, to the best of our knowledge, no analysis has been presented by other authors to date.

Until recently, the main obstacle to analysis has been the lack of an appropriate diode model: one that is not only simple enough to allow analysis but is also accurate enough to reveal the observed phenomena. Recently, however, a suitable piecewise-linear (PWL) diode model has been developed [8]. This model, used in our analysis, is shown in Fig.4. It comprises two linear capacitances, a linear resistance, and an ideal switch, whose state depends on the anode-cathode voltage. The PWL model is capable of modelling, to first order, transient effects such as reverse recovery.

In this paper we give analysis of the DH phenomenon, output voltage limits, frequency band of its appearance and the dependence of phenomenon dynamics on circuit parameters. The numerical results are verified by comparison with experimental measurements. We also determine design constraints to prevent these effects.

II. STEADY-STATE OPERATION

We first analyse steady-state operation of the rectifier in Fig.1. The analysis of *ideal operation* (without diode reverse recovery) is done with diodes modelled as ideal switches which turn on and off instantaneously. The analysis [10] gives the following expression in V_o :

$$\frac{V_o}{V_D} = -\frac{4L}{R_L T} + \sqrt{\left(\frac{4L}{R_L T}\right)^2 + 1}$$

This equation shows that at a given inductance value, the normalised output voltage depends on the drive frequency $1/T$ and the load.

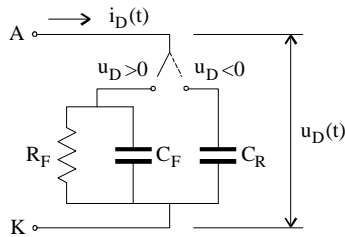


Fig.4. Simplest PWL diode model exhibiting transient behaviour.

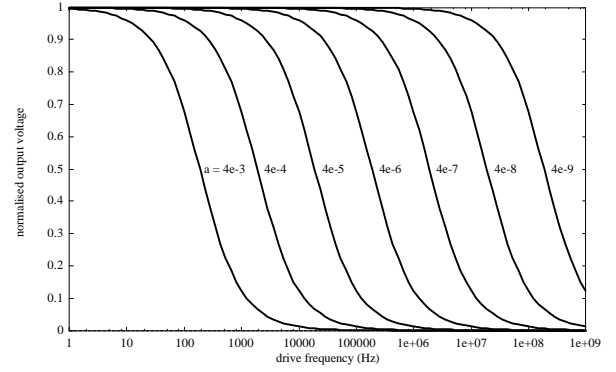


Fig. 5. Output voltage dependence on frequency for a wide range of parameter $a = 4L/R_L$.

Fig.5 shows a family of curves for a range of parameter $a = 4L/R_L$. Each curve has a value of a ten times larger than the adjacent curve, shifting it a decade higher in frequency. This is obvious from the equation as well. As expected, in ideal operation, output voltage is never greater than V_D .

In the analysis of *operation including diode reverse recovery* we employ the PWL diode model of Fig. 4 instead of ideal diodes. Fig. 6 shows a model of the converter with D_1 and D_3 conducting. Now the diodes do not switch off when the inductor current becomes negative at $t = T_1$. They conduct for an additional interval ΔT needed for stored excess minority charge carriers to be removed from the diode (reverse recovery).

The equations for this case are obtained analysing the converter waveforms and the diode reverse recovery. The system of equations can be also normalised with respect to the drive voltage V_D and the diodes' excess minority carrier recombination lifetime τ (equal to $R_F C_F$ in the PWL diode model):

$$v = \tau \cdot \frac{R_L}{L} \cdot \frac{2t_2}{T_n} \left(\frac{T_n}{2} - t_2 \right)$$

$$\Delta t = \frac{1}{2} \cdot \left[t_2 - \left(\frac{T_n}{2} - t_2 \right) \frac{1-v}{1+v} \right]$$

$$0 = [B - (1+v)(t_2 - \Delta t + 1)] \exp(-t_2) - (1+v)(\Delta t - 1)$$

where

$$B = [(1-v) - (1+v)\Delta t] \exp\left(-\frac{T_n}{2} + t_2\right) + (1-v) \left(\frac{T_n}{2} - t_2 - 1 \right) + (1+v)\Delta t$$

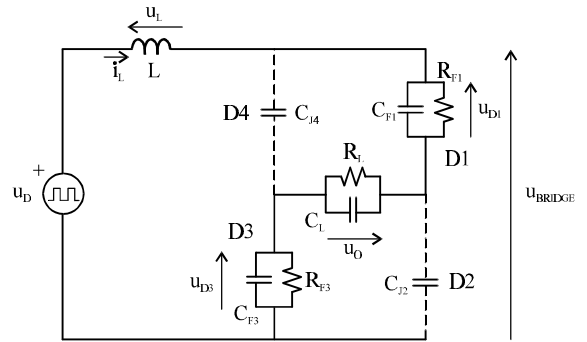


Fig. 6. Converter model with D_1 and D_3 conducting.

This normalised equations show that, out of eight circuit and diode parameters, only three qualitatively determine its behaviour: inductance L , load resistance R_L , and diode excess minority charge carrier recombination time τ . All three appear in the first equation, forming a constant that can be denoted by a parameter $A = \tau R_L/L$. This explains why the phenomenon can be observed experimentally even when fast diodes are used. If τ is small, the phenomenon appears at large load R_L and/or small L . It appears at higher frequencies, since the drive period in equations is normalised by τ . For example, Fig. 2 was measured for $L = 9.42$ mH, $R_L = 10$ k Ω and $t = 7.2$ μ s, giving $A = 7.64$, and the maximum output voltage occurred at $f = 43$ kHz. Our model predicts a similar graph and behaviour with faster diodes having $t = 1$ μ s but with $L = 100$ μ H, $R_L = 764$ Ω . The maximum would then be at $f = 310$ kHz.

The nonlinear system of equations can be solved numerically, using the Newton-Raphson method (or similar). Fig. 7 shows how the normalised output voltage depends on the normalised drive period. Unlike the ideal case in Fig.5, where the output voltage is always less than unity and decays monotonically with rising frequency, here it is greater than unity, increases to a maximum, then decays more steeply toward zero.

This results agree very well with the deviations noticed in practical converters, described above. The experimental dependence shown in Fig. 2 was obtained for circuit parameters that give $A = 7.64$, and measurements give maximum normalised output voltage value $v = 12.24/5 = 2.45$ at $T_n = 1/(43$ kHz $\cdot 7.2$ ms) = 3.23. The numerical results for the same $A = 7.64$ agree well: $v = 2.5$ and $T_n = 2.7$. This validates the simplifications made in the analysis.

Above steady-state analysis explains increased output voltage phenomenon but it does not explain the DH phenomenon—it cannot be noticed in Fig. 7. This should have been expected. In the DH phenomenon the output voltage oscillates between two levels which obviously is not a steady-state operation. That is why we need to analyse converter dynamic operation.

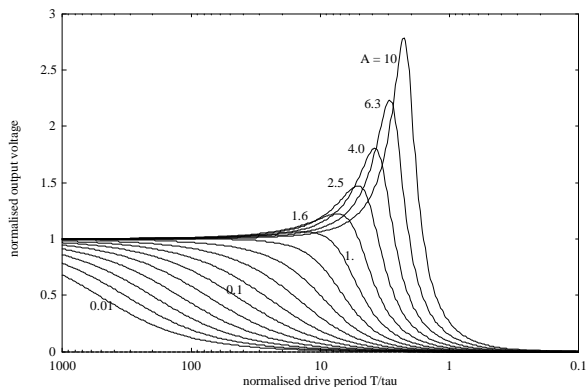


Fig. 7. Dependence of the normalised output voltage v on the normalised drive period T_n

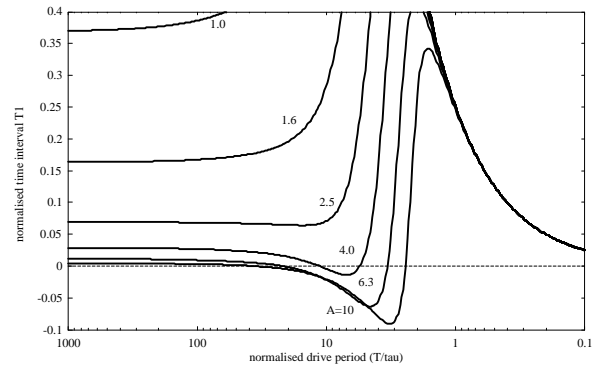


Fig. 8. Dependence of the normalised time interval T_1 on the normalised drive period T_n

III. DYNAMIC OPERATION

The reason for the instability of the steady-state conditions in the DH phenomenon can be noticed in Fig. 8. It shows the dependency of the normalised time interval T_1 on the normalised drive period. Interval T_1 becomes negative for a certain range below the frequency at which output voltage reaches its maximum.

During negative T_1 the inductor current slope is $-V_D + V_O$ instead of $+V_D + V_O$ used in the above analysis. Equations show that the new steady-state output voltage has values lower than $-V_D$. The output voltage, obviously, cannot get negative values.

Fig.9 depicts the drive frequency (or drive period) band with negative T_1 as a function of parameter A . The DH phenomenon starts to exist for $A > 3.62$ at normalised drive period $T/\tau = 7.8$ or frequency $f = 17.8$ kHz. At higher A values, the frequency band expands. The bend high frequency agrees well with measurements. For $A = 7.64$ measurements (Fig. 2) give $T_n = 1/(39.8$ kHz $\cdot 7.2$ μ s) = 3.49 and numerical results (Fig. 8) give 2.99. For the band low frequency the measured value is $T_n = 1/(2.9$ kHz $\cdot 7.2$ μ s) = 10.77 and the numerically obtained one $T_n = 27.3$. Curves for determining the band low frequency have very shallow slopes (Fig. 8) and slight displacement gives large differences in the numerical value which explains late discrepancy.

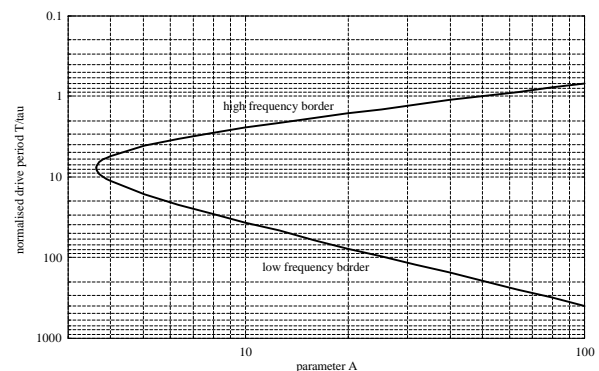


Fig.9 Frequency borders of DH phenomenon appearance as a function of parameter $A = t R_L/L$

When T_1 becomes negative, the inductor peak current starts to decrease towards zero rapidly, leading to a new regime with all diodes switched off. Converter equivalent scheme for this case is shown in Fig.10. Having in mind that C_L is large and behaves like a constant voltage source within one half-cycle, we obtain that converter small signal equivalent scheme comprises only L , C_j and eventually inductance and diodes resistances $r_D + r_L$ as shown in Fig.11.

This equivalent series-resonant circuit gets initial energy (i.e. charge in C_j) at every edge of the input pulses, and produces damped high frequency oscillations at frequency $f_0 = 1/(2\pi LC_j)^{1/2}$ noticed in Fig. 2. These oscillations are present in inductor current and bridge voltage and are shown in Fig. 12.

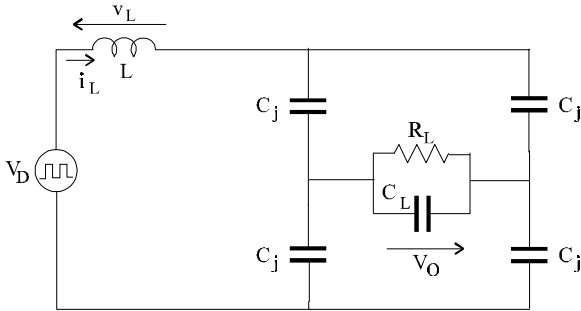


Fig.10. Converter equivalent scheme when all diodes are switched off.

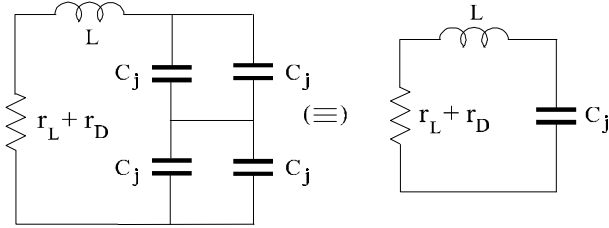


Fig.11. Converter small-signal equivalent scheme

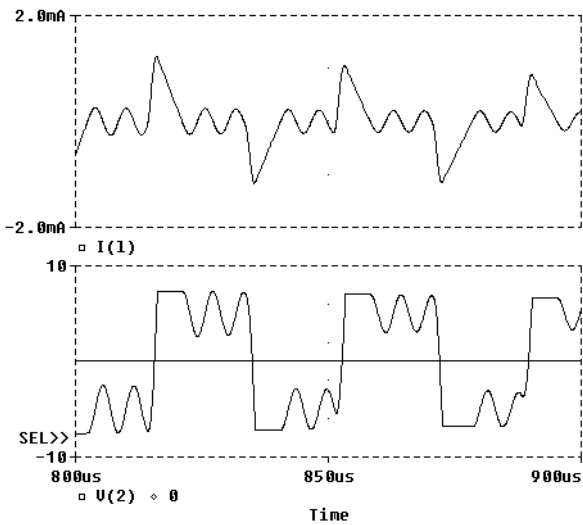


Fig. 12. High frequency oscillations produced by the series resonant circuit comprising L , C_j and $r_D + r_L$: (a) inductor current, and (b) bridge voltage

Due to the symmetry in the circuit, an equal current (a half of the inductor current) flows through each junction capacitance in the bridge. This current does not pass through load and output filter capacitor and they form an independent RC circuit shown in Fig. 13. Thus the output voltage v_O decreases exponentially to zero. This decay continues until v_O becomes lower than drive voltage V_D . Then conditions for diodes to conduct exist again, and the voltage starts to rise to its unstable steady-state value, few times higher than V_D . This exponential decay of the output voltage and the amplitude of the bridge pulses and shown in Fig. 14. The decay time interval is equal to $\tau \cdot \ln(V_{max} / V_D)$ and depends on recombination lifetime and initial pulses voltage V_{max} .

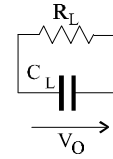


Fig.13. RC circuit formed by the converter load and filter capacitance

Voltage and current waveforms while v_O rises are shown in Fig. 15. Iterative equations that describe this process can be obtained in a similar way as in the steady state case from the waveforms in Fig. 15 and analysing the charging and discharging process of the diode model capacitance C_F . The equations are:

$$\Delta v(n) \frac{1}{AB} = \left\{ i_{D0}(n) + \frac{1-v(n)}{2} \left[\frac{T_n}{2} - t_2(n-1) \right] - \frac{v(n)}{A} \right\} \cdot \left[\frac{T_n}{2} - t_2(n-1) + t_2(n) \right] - \frac{1-v(n)}{2} \left[\frac{T_n}{2} - t_2(n-1) \right] - \frac{1+v(n)}{2} t_2^2(n) - i_{D0}(n+1) = i_{D0}(n) + [1-v(n)] \left[\frac{T_n}{2} - t_2(n-1) \right] - [1+v(n)] t_2(n)$$

and

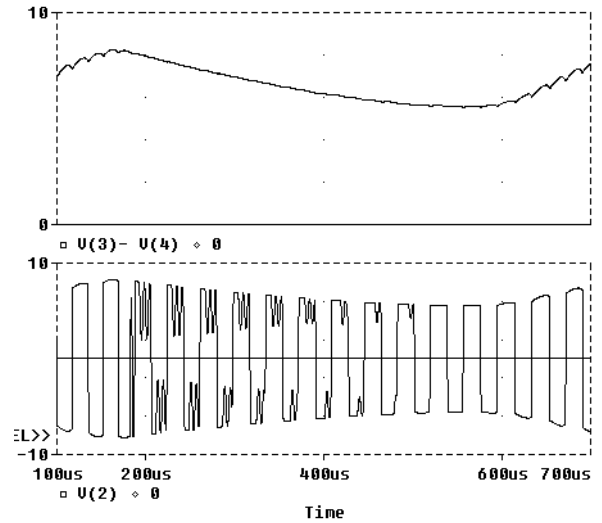


Fig. 14. Exponential decay of: (a) the output voltage, and (b) the amplitude of the bridge pulses.

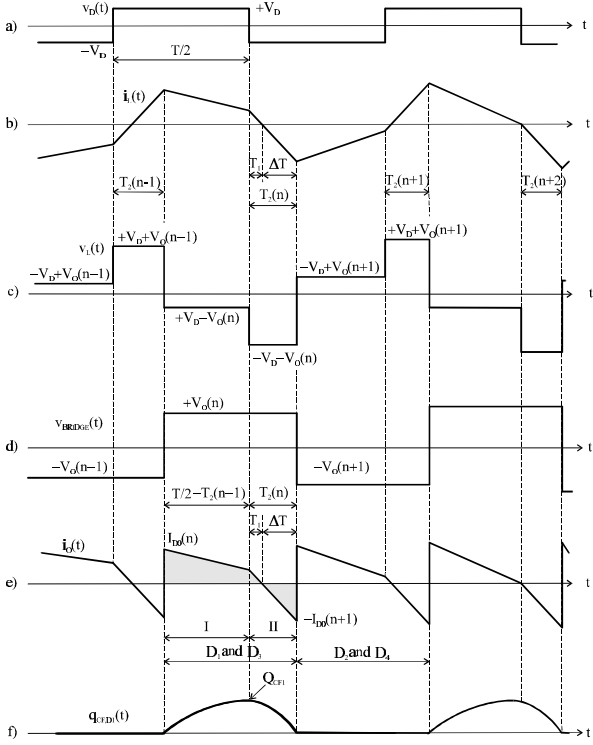


Fig. 15 Converter waveforms in non steady-state case: a) drive voltage, b) inductor current, c) inductor voltage, d) bridge voltage, e) output current and f) diode model capacitance C_F charge.

$$0 = \left\{ Q_{CF1} \frac{L}{V_D \tau^2} - i_{D0}(n) - [1 - v(n)] \left[\frac{T_n}{2} - t_2(n-1) \right] - 1 - v(n) \right\} \exp[-t_2(n)] - [1 + v(n)] t_2(n) + i_{D0}(n) + [1 - v(n)] \left[\frac{T_n}{2} - t_2(n-1) \right] + 1 + v(n)$$

where

$$Q_{CF1} \frac{L}{V_D \tau^2} = [-i_{D0}(n) + 1 - v(n)] \exp \left[-\frac{T_n}{2} + t_2(n-1) \right] + i_{D0}(n) + [1 - v(n)] \left[\frac{T_n}{2} - t_2(n-1) - 1 \right]$$

and n is the n -th half-cycle starting from the instant when $v_O = V_D$.

These equations show that four circuit parameters determine the circuit dynamic behaviour: L , R_L , C_L and τ . All of them appear in the first equation, forming two constants. The first one is the same as in the steady-state case, $A = \tau \cdot R_L / L$. The second one is new and includes output filter capacitance, $B = \tau / (C_L \cdot R_L)$. Both constants relate the recombination lifetime τ with the time constants formed by L and C_L .

Numerical results of these iterative equations are shown in Figs. 16 and 17. Fig. 16 shows the dependence of the normalised output voltage rise towards its steady-state value on parameter A . Other parameters are $T_n = 5.14$ ($f = 27$ kHz) and $B = 11.7 \cdot 10^{-3}$, and they are obtained from the parameters of the converter used for the measurements in Fig. 2. Each adjacent curve is obtained for 1.096 times higher parameter A and only

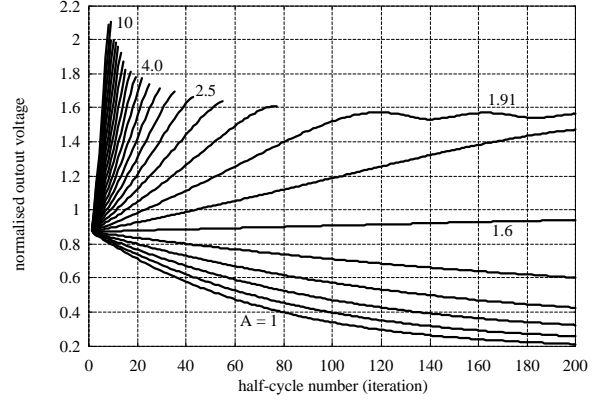


Fig. 16. Dependence of the normalised output voltage rise on the parameter A ($T_n = 5.14$ and $B = 11.7 \cdot 10^{-3}$)

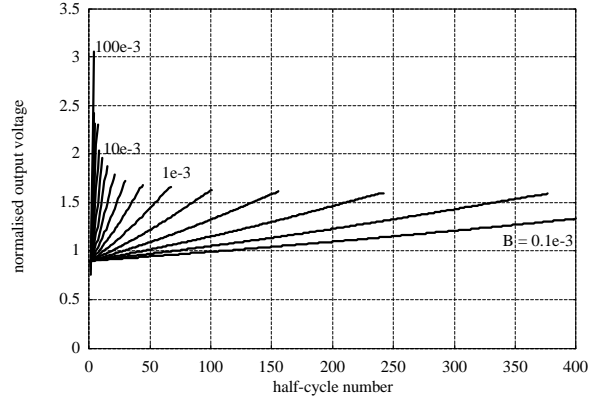


Fig. 17. Dependence of the normalised output voltage rise on the parameter B ($T_n = 5.14$ and $A = 7.64$)

the first 200 iterations are shown since they are sufficient to determine converter behaviour. At low A values the output voltage v_O exponentially approaches its steady state value. This is true until A equals 1.91 when it undergoes oscillatory transients. For higher A values, the v_O significantly overshoots the steady state. These curves are truncated when T_1 becomes negative, since then voltage rise regime ends, and all diodes switch off. Voltage v_O starts to decay exponentially again as explained above. The number of iterations before this happens is in correspondence with measurements: for $A = 7.64$ the rise ends after 11 half-cycles and v_O reaches value 1.96 which agrees very well with Fig. 2.

Fig. 17 shows the dependence of the normalised output voltage rise on the parameter B , i.e. output filter capacitance C_L at $A = 7.64$ and $T_n = 5.14$. As this figure shows, parameter B determines the speed of reaching the maximum voltage level. For low B values there are no evident overshoots. For B roughly greater than $1 \cdot 10^{-3}$ the slope is very steep, overshooting is significant and v_O reaches much higher values than predicted by steady-state analysis.

IV. DESIGN CONSIDERATIONS

Fig. 7 shows that the output voltage V_O becomes higher than the drive voltage V_D only when A becomes greater than

unity (approximately). This overvoltage can be several times higher than V_D at higher A values, i.e. at light loads or with slow diodes, and might destroy output filter capacitors, usually designed for $V_O \leq V_D$. To avoid overvoltages and strange behaviour, the series-resonant converter and high-frequency rectifiers should be designed so that even in the worst case, i.e. at lightest loads, the condition $A = \tau R_L/L \leq 1$ is satisfied, giving:

$$\frac{L}{R_{L,MAX}} \geq \tau$$

For example, the parameters used for Fig. 2 give the circuit time constant $L/R = 9.42 \text{ mH}/10\text{k}\Omega = 0.942 \mu\text{s}$, the diode time constant $\tau = 7.2 \mu\text{s}$ and $A = 7.2/0.942 = 7.64$. To make A less than unity we need to increase L/R , by decreasing R , increasing L , or adjusting both simultaneously.

If the circuit parameters are given, Fig. 7 and the above relation can be used to determine the maximum switching frequency above which the output voltage decreases below allowable limits, e.g. by 10% or less. For this purpose, the voltage axis of Fig. 18 employs a log scale for improved legibility. On the other hand, if the switching frequency is known, Fig. 18 gives the minimum A value for the same criterion. Hence the maximum allowable inductance at the input of the bridge rectifiers can be determined. This condition should be met even for the worse case, i.e. for the minimum value of R_L .

Fig. 17 shows that parameter B can further increase output voltage significantly above its steady-state value if $B = \tau/(C_L R_L) > 1 \cdot 10^{-3}$ i.e. if output voltage rises very steep. To avoid this, a correct design should also take care of an additional constraint on the output filter capacitor:

$$C_L > \frac{\tau}{10^{-3} R_{L,MIN}}$$

The above relations are also useful for the series-resonant converter, since at high frequencies its behaviour is similar. These constraints should be added to the design rules for series-resonant converters [3, p. 405], and are further reason for adding a pre-load at the output. Also, the correct frequency range for regulating the output voltage can be determined from Fig. 18.

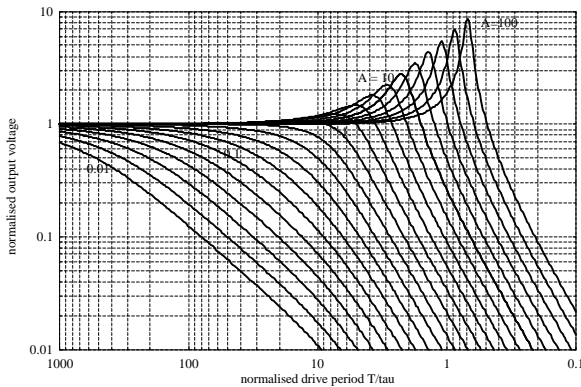


Fig. 18. Dependence of the normalised output voltage v on the normalised drive period T_n

V. CONCLUSION

Diode reverse recovery affects the operation of high-frequency rectifiers. The deviations from ideal operation can produce substantial overvoltages and quasi-periodic oscillation, open-loop. The equations derived clearly show that the phenomena depend on $A = \tau R_L/L$ and $B = \tau/(C_L R_L)$, i.e. on only four out of eight circuit parameters. These are: (1) diode excess minority charge carrier recombination time; (2) converter load resistance; (3) source inductance; and (4) output filter capacitance. Comparison with experimental measurements shows close agreement. When faster diodes are used, the same effects will be observed but at higher frequencies.

Two additional constraints, $A < 1$ or $L/R_{L,MAX} > \tau$, and $B > 1 \cdot 10^{-3}$ or $C_L > \tau/(1 \cdot 10^{-3} R_{L,MIN})$ should be added to the design rules for converters, in order to protect the circuit from overvoltages (which might damage output filter capacitors) and from open-loop instability (quasiperiodicity). For frequency-controlled converters, a modified frequency range should be used, and this can be determined from the graphs presented.

This work can form the basis for analysing similar phenomena in other converters. All switching converters have some stray inductance in series with their diodes, so we expect the phenomena to be widespread, especially as switching frequencies are pushed ever higher. Further investigations should explain a general influence of delay, and similar effects in switching converters where the duty ratio is not 0.5. Analysis of appropriate control methods and their closed-loop stability are also of interest. These and other investigations are made possible now a suitable piecewise-linear diode model is available.

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