

# Class DE Inverters and Rectifiers for DC-DC Conversion

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**Abstract** — A new family of Class DE inverters and related rectifiers is presented. Based on the Class D rf inverter, the circuits feature Class E switching transitions (zero voltage, zero  $dv/dt$ ), giving low switching losses despite device capacitance and stored charge, combined with low voltage stress. Matching between inverter and rectifier is considered, time reversal duality is introduced, and a family of inverters and rectifiers is presented. The circuits should find application in megahertz dc-dc converters.

## I INTRODUCTION

This paper describes a family of inverters and rectifiers featuring zero voltage, zero  $dv/dt$  switching. The inverters are a hybrid between the Class D and Class E rf amplifiers. Their switches turn on at zero voltage and zero  $dv/dt$ , giving low switching losses despite intrinsic device capacitance. The rectifier waveforms are time reversed versions of the corresponding inverter waveforms. The rectifier diodes start to block under conditions of zero voltage and zero  $dv/dt$ ; thus diode capacitance and charge storage do not have a deleterious effect.

After a brief description of Class D, E and DE rf power amplifiers, a half bridge Class DE inverter is studied from a theoretical standpoint. Next the corresponding Class DE rectifier is introduced and analysed in a similar way. To form a Class (DE)<sup>2</sup> dc-dc converter the inverter and rectifier must be combined, and the matching requirements are examined. The concept of time reversal duality is briefly introduced, then some more Class DE inverter and rectifier topologies are presented. The circuits should be suitable for use in dc-dc converters with megahertz switching frequencies.

## II CLASSES D, E, AND DE

The purpose of a radio frequency power amplifier is to deliver, with reasonable efficiency, a sinusoidal signal having low harmonics and other spurious components. Rf power amplifiers are classified by the operation of their output transistors. Classes A to C use transistors in the active region, so they are

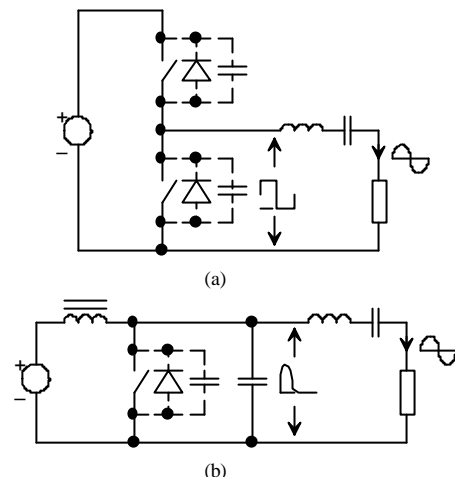


Fig. 1: (a) Class D and (b) Class E inverters, showing parasitic switch capacitances and diodes

generally unsuitable for use in power converters, where efficiency is far more important than signal purity.

To increase efficiency, the transistors may instead be operated as switches. The earliest example, now known as Class D, dates from 1959 [1]. Shown in Fig. 1(a), it is a two-switch topology in which the switches conduct on alternate half cycles, each with a conduction angle approaching 180°. A series resonant tank converts the square voltage waveform into a sinusoidal load current. The transistors operate with zero current switching (ZCS), turning on and off as the load current crosses zero. The Class D amplifier is familiar in a power conversion context as the voltage fed half bridge series resonant inverter.

Although it is theoretically 100% efficient, in practice Class D suffers from switching loss because the inherent device capacitances must be charged and discharged every switching cycle, dissipating energy and thus reducing efficiency. The effect worsens at higher frequencies, until the low losses expected from ZCS are no longer achieved.

Class E, shown in Fig. 1(b), was introduced in 1975 [2]. It overcomes the device capacitance problem by means of zero

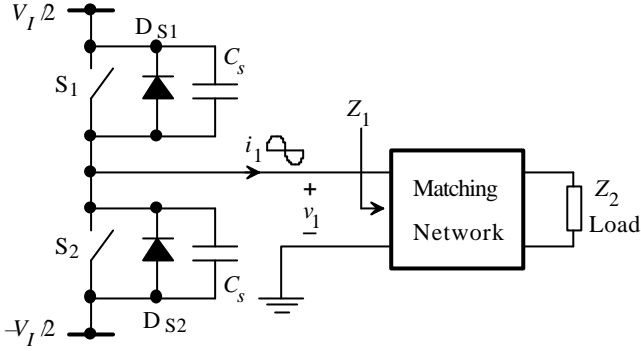


Fig. 2: Half bridge Class DE inverter circuit

voltage switching (ZVS). The switch is turned on only when its shunt capacitance has been discharged by the surrounding circuit. (More recently, ZVS has been widely applied to quasi-resonant dc-dc converters.) However, in true Class E operation the switch also closes when  $dv/dt = 0$ , giving low sensitivity to the circuit parameters and switching times.

A disadvantage of the current fed Class E circuit is that it imposes a much higher peak voltage stress on the switches than the voltage fed Class D: in optimum Class E operation the stress is 3.6 times the dc input voltage [3], compared to unity for Class D. Both circuits see similar peak currents.

A hybrid combining the best features of Class D and Class E operation was first proposed by Zhukov and Kozyrev in 1975 [4], but their work was unknown in the West. In this hybrid the sinusoidal output current swings the voltage from one dc rail to the other during a short dead time when both switches are open. Steigerwald [5] noted the use of zero voltage switching in Class D, but did not analyse it. Recently the Zhukov–Kozyrev circuit was rediscovered by Koizumi et al. [6–8]. They employed a duty factor of 25%, and coined the term *Class DE* for its zero voltage, zero  $dv/dt$  switching. The circuit was also investigated independently by El-Hamamsay [9], and a generalised version of the amplifier (with arbitrary duty factor) was analysed by Hamill [10].

### III. HALF BRIDGE CLASS DE INVERTER

Fig. 2 shows the circuit of a half bridge Class DE inverter which will be studied in detail. For convenience the dc input is shown as a centre tapped supply. An ideal switch, a diode and a capacitor model each of the two switching devices (in practice, probably MOSFETs). The capacitor includes the device capacitance plus any additional external capacitance. A high  $Q$  matching network forces the inverter's output current waveform to be almost sinusoidal.

#### A. Operation

Fig. 3 shows the inverter's waveforms. With each switch shunted by capacitance  $C_s$ , the total capacitance  $2C_s$  is charged by the negative output current  $i_1$  when switch  $S_2$

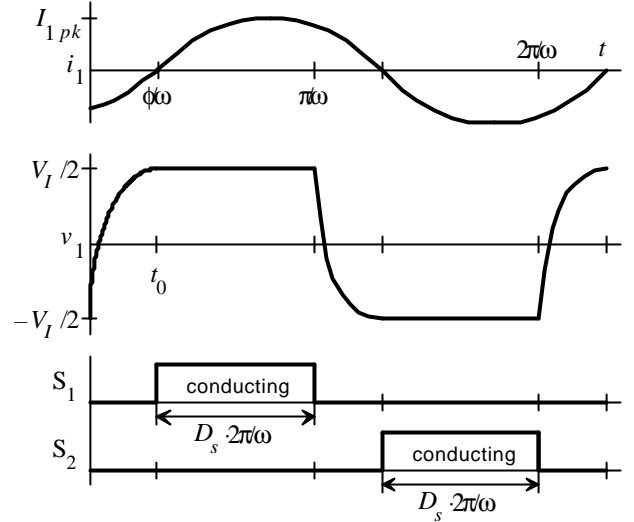


Fig. 3: Waveforms of the Class DE inverter

opens at  $t = 0$ . The inverter's output voltage  $v_1$  rises from the negative rail towards the positive rail, which it reaches at time  $t_0$ . Diode  $D_{S1}$  prevents  $v_1$  from rising further, and  $S_1$  is turned on with ZVS at  $t_0$ . The other half cycle is similar.

#### B. Analysis

Let the dc input voltages be  $\pm V_I/2$  and the inverter's output current be  $i_1(t) = I_{1pk} \sin(\omega t - \phi)$ , where  $\omega/2\pi$  is the switching frequency and  $\phi \in [0, \pi]$  is a phase angle. ( $I_{1pk}$  and  $\phi$  both depend on the matching network and the load impedance.) For Class E transitions,  $dv_1/dt = 0$  at  $t_0$ . Since  $dv_1/dt = -i_1/2C_s$ ,  $i_1(t_0) = 0$  so  $\phi = \omega t_0$ . If each switch operates with a duty factor  $D_s \in [0, 1/2]$ , then from Fig. 3,  $D_s = (\pi - \phi)/2\pi$ . To swing  $v_1$  from  $-V_I/2$  to  $V_I/2$ , the total switch capacitance  $2C_s$  must be supplied with charge  $2C_s V_I = \int -i_1(t) dt$ . Integrating and solving for  $I_{1pk}$ ,

$$I_{1pk} = \frac{2\omega C_s V_I}{1 - \cos \phi} \quad (1)$$

(Note that a small phase angle  $\phi$  implies a large peak current.) Substituting for  $i_1$  in  $dv_1/dt = -i_1/2C_s$  and integrating,

$$v_1(t) = V_I \frac{2 \cos(\omega t - \phi) - (1 + \cos \phi)}{2(1 - \cos \phi)}, \quad t \in [0, t_0] \quad (2)$$

In Class E analysis an effective impedance approach is often used. Moreover, the quantities are usually normalised with respect to a reference impedance (usually the reactance of the switch capacitance). That approach is adopted here: current  $i_1(t)$  is represented by a phasor,  $\mathbf{I}_1$ , and the fundamental component of voltage  $v_1(t)$  is represented by another phasor,  $\mathbf{V}_1$ . (Only the fundamental need be considered, as the high  $Q$  matching network rejects harmonics.) Hence an effective load impedance  $\mathbf{Z}_1 = \mathbf{V}_1/\mathbf{I}_1$  can be calculated.

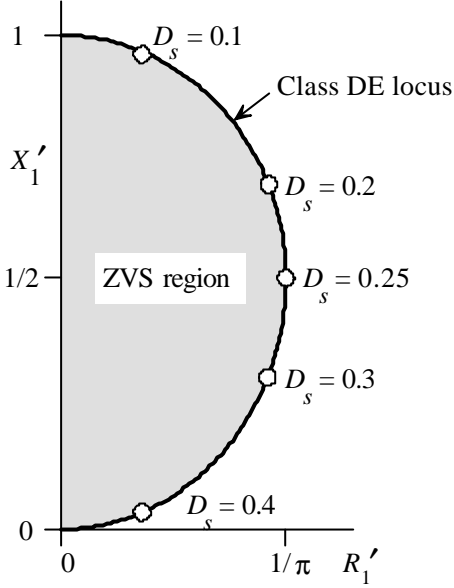


Fig. 4: Normalised effective load impedance plane (NELIP) for the Class DE inverter

The fundamental components of  $v_1(t)$  and  $i_1(t)$  can be found by Fourier analysis. Suppose some quantity  $a$  is periodic with period  $2\pi/\omega$ :  $a(t) = f_\omega(t)$ . Its fundamental component can be expressed as the phasor  $\mathbf{A} = \frac{\omega}{\pi} \int_0^{2\pi/\omega} f_\omega(t) e^{-j\omega t} dt$ . Since  $v_1(t)$  has similar positive and negative half cycles, the phasor representing it is found as

$$\begin{aligned} \mathbf{V}_1 &= 2 \cdot \frac{\omega}{\pi} \left( \int_0^{\phi/\omega} v_1(t) e^{-j\omega t} dt + \int_{\phi/\omega}^{\pi/\omega} \frac{V_1}{2} e^{-j\omega t} dt \right) \\ &= V_1 \frac{\phi \cos \phi - \sin \phi - j\phi \sin \phi}{\pi(1 - \cos \phi)} \end{aligned} \quad (3)$$

Similarly,  $i_1(t)$  can be represented by

$$\begin{aligned} \mathbf{I}_1 &= 2 \cdot \frac{\omega}{\pi} \int_0^{\pi/\omega} I_{1pk} \sin(\omega t - \phi) e^{-j\omega t} dt \\ &= \frac{-2\omega C_s V_1 (\sin \phi + j \cos \phi)}{1 - \cos \phi} \end{aligned} \quad (4)$$

The effective impedance seen by the inverter is  $\mathbf{Z}_1 = \mathbf{V}_1 / \mathbf{I}_1 = R_1 + jX_1$ , say. Further,  $\mathbf{Z}_1$  is normalised by multiplying by  $2\omega C_s$  to give the dimensionless quantities

$$R'_1 = \frac{\sin^2 \phi}{\pi}, \quad X'_1 = \frac{\phi - \sin \phi \cos \phi}{\pi} \quad (5)$$

Normalisation is denoted by a prime ( $'$ ). The complex plane spanned by the real and imaginary components of  $\mathbf{Z}_1$ , i.e. the  $R'_1 - X'_1$  plane, will be designated the *normalised effective load impedance plane* (NELIP). Equations (5) describe parametrically the locus of Class DE operation in the NELIP; see Fig. 4. (The locus can be shown to be a cycloid, the curve traced out by a point on the circumference of a circle of radius  $1/2\pi$  as it

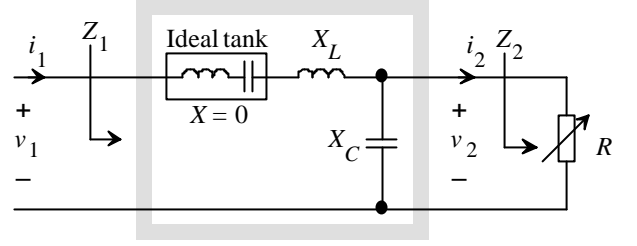


Fig. 5: Matching network for variable resistive load

rolls on the  $X'_1$  axis.) Values of the required duty factor  $D_s$  are also marked, from  $D_s = (\pi - \phi)/2\pi$ . Class DE waveforms have been verified by simulation and experimental measurement at various points on the locus.

### C. Modes of Operation

The effective load impedance applied to the inverter affects its mode of operation. Suppose that  $I_{1pk} = \alpha I_{1pk(DE)}$ , where  $I_{1pk(DE)}$  is the critical value of  $I_{1pk}$  given by (1), and  $\alpha > 0$ .

If  $\mathbf{Z}_1$  is too large,  $I_{1pk}$  will be less than the critical value ( $\alpha < 1$ ). Then  $v_1(t)$  will peak before it reaches  $V_1/2$  and fall back, so ZVS will not be obtained. This inefficient mode of operation occurs everywhere in the NELIP except for the region bounded by the Class DE locus and the  $X'_1$  axis.

On the other hand, with small values of  $\mathbf{Z}_1$ ,  $I_{1pk}$  will be greater than the critical value ( $\alpha > 1$ ). The transitions become ordinary ZVS ( $dv_1/dt \neq 0$ ). This operation occurs within the region of the NELIP bounded by the Class DE locus and the  $X'_1$  axis. Now  $v_1(t)$  reaches  $V_1/2$  while  $i_1(t)$  is still negative, forcing diode  $D_{s1}$  to conduct, at an angle  $\psi$  given by

$$\psi = \phi - \cos^{-1} \frac{1 + (\alpha - 1) \cos \phi}{\alpha} \quad (6)$$

The diode comes out of conduction when  $i_1(t)$  reaches zero, at an angle  $\phi$  as before. There is therefore some latitude in the switch turn-on angle, which may be between  $\psi$  and  $\phi$ .

In the critical case of true Class DE operation ( $\alpha = 1$ ),  $\psi = \phi$  so there is theoretically no latitude. Nevertheless,  $v_1(t)$  stays close to  $V_1/2$  for some time ( $dv_1/dt \approx 0$ ), so the exact turn-on instant is not critical — a quintessential property of Class E inverters.

### D. Matching Network

A matching network is placed between the inverter and its load impedance,  $\mathbf{Z}_2 = \mathbf{V}_2 / \mathbf{I}_2$ . This network has two functions:

- 1) it forces the inverter's load current to be nearly sinusoidal, usually by including a series resonant tank;
- 2) for any given value of  $\mathbf{Z}_2$  it should ideally give a value of  $\mathbf{Z}'_1$  lying within the efficient region of the NELIP.

Suppose the inverter is operated with a resistive load  $\mathbf{Z}'_2 = R'$ . The matching network maps each value of  $R'$  to a

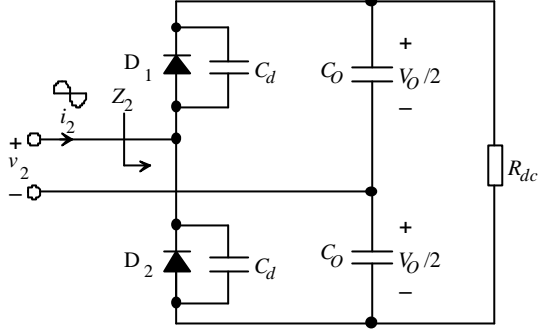


Fig. 6: Half bridge Class DE rectifier circuit

point in the NELIP. If the matching network contains only reactive elements, then when  $R = 0$  and  $R = \infty$ ,  $Z'_1$  will be purely reactive too, i.e. the ends of the locus will lie on the  $X'_1$  axis. With proper design, the whole of the locus can be made to lie within the ZVS area.

Fig. 5 shows an example of a simple  $LC$  matching network. Suitable normalised reactance values are  $X'_L = (\pi + 2)/2\pi$ ,  $X'_C = -2/\pi$ . With a short circuit,  $R' = 0$  maps to  $Z'_1 = 0.8183j$ . As  $R'$  increases, the locus moves away from the  $X'_1$  axis until it reaches  $Z'_1 = 1/\pi + 1/2j$  (on the Class DE locus) when  $R' = 2/\pi$ . It then moves back until, with an open circuit,  $Z'_1 = 0.1817j$ . Thus the locus stays within the ZVS region of the NELIP, close to the Class DE locus, permitting efficient operation with any value of resistive load.

#### E. Switch Utilisation

A utilisation factor for the switches in an ideal power converter may be defined by  $U = P/(V_{\max} I_{\max} n)$ , where  $P$  is the power throughput, and  $V_{\max}$  and  $I_{\max}$  are the voltage and current stresses on each of the  $n$  switches.  $U$ , which lies between 0 and 1, is useful for comparing diverse topologies. For Class DE,

$$P = \frac{1}{2} \text{Re } \mathbf{V}_1 \mathbf{I}_1^* = \frac{V_1^2 \omega C_s}{\pi} \cdot \frac{1 + \cos \phi}{1 - \cos \phi} \quad (7)$$

Also  $V_{\max} = V_1$ ,  $I_{\max} = I_{1pk}$ , given by (1), and  $n = 2$ . Hence  $U = (1 + \cos \phi)/4\pi$ . Its best value,  $U = 0.159$ , is obtained when  $\phi = 0$  ( $D_s = 0.5$ : classical Class D). The optimum Class E inverter has  $U = 0.098$  [3], which the Class DE inverter betters with  $D_s > 0.29$ . In summary, with low voltage stress, low switching loss and acceptable switch utilisation, the Class DE circuit is an attractive inverter for high frequency operation.

## IV. HALF BRIDGE CLASS DE RECTIFIER

The need for rectifiers with smooth switching transitions and ZVS has been acknowledged by other workers, e.g. [11, 12]. The rectifier of Fig. 6 is a close relative of the half bridge Class DE inverter [13]. It too is insensitive to capacitive effects,  $C_d$  subsuming the junction capacitance and diffusion

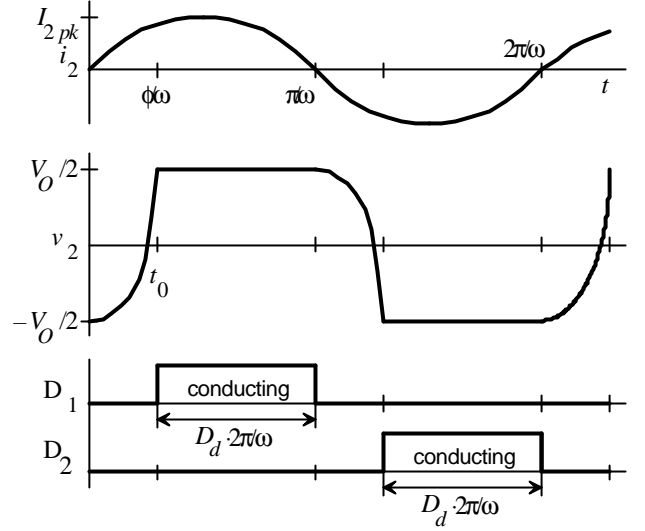


Fig. 7: Waveforms of Class DE rectifier

charge storage that plague real rectifier diodes at high frequencies.

#### A. Operation

It is assumed that the circuit is fed by a sinusoidal current, the diodes are ideal, the two capacitances  $C_d$  are ideal and linear, and the two output capacitances  $C_o$  are infinite. By symmetry, each  $C_o$  carries an equal voltage. The dc load is a resistance  $R_{dc}$ .

Refer to Fig. 7 for waveforms. At  $t = 0$ , the input current  $i_2$  becomes positive and  $D_2$ , which was previously conducting, starts to block. The current therefore diverts to charge the total diode capacitance  $2C_d$ . At  $t = 0$ ,  $dv_2/dt = 0$ , giving a Class E transition. The input voltage  $v_2$  starts to rise from the negative output rail to the positive one, which it reaches at  $t_0$ . Then  $D_1$  comes into conduction, and remains conducting until  $i_2$  changes sign again. The other half cycle is similar.

#### B. Analysis

Let the input current  $i_2(t) = I_{2pk} \sin \omega t$ , and let the voltage across each output capacitor  $C_o$  be  $V_o/2$ .

Integrating  $dv_2/dt = i_2/2C_d$  and using the fact that  $v_2(0) = -V_o/2$ , voltage  $v_2$  is found as

$$v_2(t) = \frac{I_{2pk}}{2\omega C_d} (1 - \cos \omega t) - \frac{V_o}{2} \quad (8)$$

At  $t = 0$ ,  $dv_2/dt = i_2/2C_d = 0$  (Class E). The transition ends at  $t = t_0$ , when  $v_2(t_0) = V_o/2$ . Writing  $\phi = \omega t_0$ , from (8) we have

$$\cos \phi = 1 - \frac{2\omega C_d V_o}{I_{2pk}} \quad (9)$$

From Fig. 7 it can be seen that the duty factor of each diode is  $D_d = (\pi - \phi)/2\pi$ , lying between 0 and  $1/2$ .

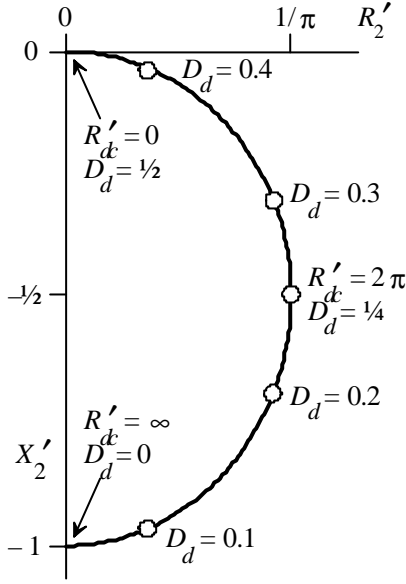


Fig. 8: Normalised effective input impedance of the Class DE rectifier

It is useful to know the effective input impedance of the rectifier at the input current frequency. Using Fourier analysis as for the inverter, in phasor form  $v_2(t)$  and  $i_2(t)$  become

$$\begin{aligned} \mathbf{V}_2 &= 2 \cdot \frac{\omega}{\pi} \left( \int_0^{\phi/\omega} v_2(t) e^{-j\omega t} dt + \int_{\phi/\omega}^{\pi/\omega} \frac{V_O}{2} e^{-j\omega t} dt \right) \\ &= V_O \frac{\sin \phi \cos \phi - \phi - j\phi \sin^2 \phi}{\pi(1 - \cos \phi)} \end{aligned} \quad (10)$$

and

$$\begin{aligned} \mathbf{I}_2 &= 2 \cdot \frac{\omega}{\pi} \int_0^{\pi/\omega} I_{2pk} \sin \omega t e^{-j\omega t} dt \\ &= -jI_{2pk} \end{aligned} \quad (11)$$

Substituting for  $I_{2pk}$  from (9) into (11), the effective input impedance is found as  $\mathbf{Z}_2 = \mathbf{V}_2/\mathbf{I}_2$ . After normalisation (now using  $2\omega C_d$ ) this becomes

$$\mathbf{Z}'_2 = 2\omega C_d \mathbf{Z}_2 = \frac{\sin^2 \phi + j(\sin \phi \cos \phi - \phi)}{\pi} \quad (12)$$

Therefore the normalised resistance and reactance are

$$R'_2 = \frac{\sin^2 \phi}{\pi}, \quad X'_2 = \frac{\sin \phi \cos \phi - \phi}{\pi} \quad (13)$$

As for the inverter, varying  $\phi$  traces out a cycloidal locus in the  $\mathbf{Z}'_2$  plane. This is shown in Fig. 8, with several values of the diode duty factor  $D_d$  also marked.

Often it is convenient to work in terms of the circuit quantities, as determined next. The charge flowing through  $D_1$  into the upper  $C_o$  reservoir capacitor during a cycle is

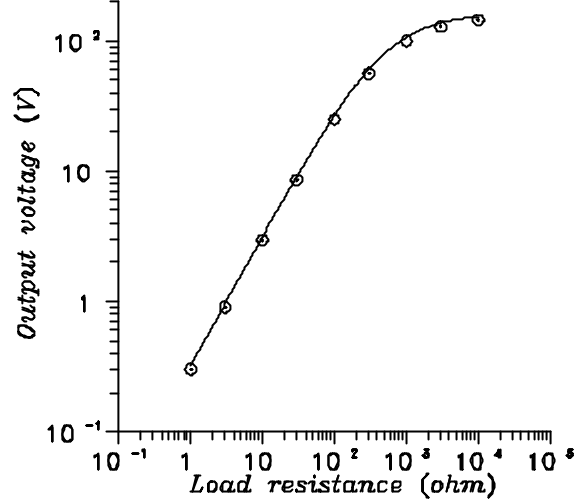


Fig. 9: Plot of rectifier output voltage  $V_o$  as a function of load resistance  $R_{dc}$ . Line: theory; points: PSpice simulation with non-ideal diodes

$$Q_1 = \int_{\phi/\omega}^{\pi/\omega} i_2(t) dt = \frac{2I_{2pk}}{\omega} - 2C_d V_O \quad (14)$$

(Additional charge flows in via the diode capacitances during the interval  $[0, \phi/\omega]$ , but an equal amount flows out during  $[\pi/\omega, (\pi + \phi)/\omega]$ , cancelling out.) The charge flowing through  $R_{dc}$  during a cycle is  $Q_2 = (2\pi/\omega)V_O/R_{dc}$ . In the steady state,  $Q_1 = Q_2$ ; hence  $I_{2pk} = V_O(\pi/R_{dc} + \omega C_d)$ . Substituting into (9) and using the identity  $\sin^2 \phi + \cos^2 \phi = 1$ ,

$$\cos \phi = \frac{\pi - \omega C_d R_{dc}}{\pi + \omega C_d R_{dc}}, \quad \sin \phi = \frac{\sqrt{4\pi\omega C_d R_{dc}}}{\pi + \omega C_d R_{dc}} \quad (15)$$

Writing  $R'_{dc} = 2\omega C_d R_{dc}$ , (13) yields

$$R' = \frac{8R'_{dc}}{(2\pi + R'_{dc})^2} \quad (16)$$

and

$$X'_2 = \sqrt{\frac{8R'_{dc}}{\pi}} \cdot \frac{2\pi - R'_{dc}}{(2\pi + R'_{dc})^2} - \frac{1}{\pi} \cos^{-1} \frac{2\pi - R'_{dc}}{2\pi + R'_{dc}} \quad (17)$$

Values of  $R'_{dc}$  are included in Fig. 8.

Finally, from (9) the total output voltage may be found as

$$V_O = \frac{I_{2pk} R_{dc}}{\pi + \omega C_d R_{dc}} \quad (18)$$

### C. Modes of Operation

Unlike the inverter, in which there are three operating modes, the rectifier has only a single mode of operation: Class DE. Whereas the inverter switches can be turned on or off at

any desired instant, the diodes, acting as passive switches, have no such freedom: their switching operation is constrained by the voltages and currents in the surrounding circuit to be Class DE, with the requisite duty factor.

#### D. Simulation Results

PSpice simulations were performed to verify the analysis. With  $I_{2pk} = 1\text{A}$ ,  $\omega/2\pi = 1\text{MHz}$  and  $C_d = 1\text{nF}$ , non-ideal diodes were modelled by the statement `.MODEL DIODE D(IS=100f RS=10m Cj0=100p Tt=50n)`. (The diode capacitance was additional to the external  $C_d$ .) Lead inductance of  $10\text{nH}$  was put in series with each diode. Fig. 9 shows good agreement between (18) and the simulation results over four decades of load resistance. This being a current fed rectifier, the diode conduction voltage does not affect the output voltage.

### V. MATCHING INVERTER AND RECTIFIER

It is interesting to consider a Class DE inverter driving a Class DE rectifier, forming what might be termed a *Class (DE)<sup>2</sup> dc-dc converter*.

Compare the required load impedance locus for the inverter,  $\mathbf{Z}'_1$  (Fig. 4), with the input impedance locus of the rectifier,  $\mathbf{Z}'_2$  (Fig. 8). They are the same size and shape, but differ by  $X' = 1$ . In the special case where  $C_s = C_d$ , the design of the matching network is particularly simple. Apart from the series resonant tank tuned to  $\omega$ , all that is needed is additional series inductance providing reactance  $X'_L = 1$ . This will shift the rectifier's impedance locus vertically so it exactly overlies the Class DE locus in the inverter's NELIP. In practice, the extra inductive reactance can be obtained simply by increasing the inductance in the series tank circuit; the matching network simply consists of  $L$  and  $C$  in series.

Subject to the approximations made in the analysis, this matching network will allow Class DE operation of both the inverter and the rectifier, no matter what the rectifier's dc load. If the inverter's duty factor is properly chosen, both the inverter and the rectifier will enjoy low switching losses.

Transformer coupling with an arbitrary primary-to-secondary turns ratio  $N_1 : N_2$  is also possible. The values of  $C_s$  and  $C_d$  must be correctly chosen, viz. to satisfy

$$\frac{C_d}{C_s} = \left(\frac{N_1}{N_2}\right)^2 \quad (19)$$

The transformer's leakage inductance can be absorbed into the series tank circuit, while its magnetising inductance can be cancelled by adding a shunt capacitor to resonate at  $\omega$ .

The Class (DE)<sup>2</sup> dc-dc converter is a promising candidate for megahertz dc-dc conversion. Possible methods for controlling the output include frequency modulation, asymmetric PWM, phase shift control, and synchronous rectification.

### VI. TIME REVERSAL DUALITY

As evidenced by Figs. 3 and 7, the waveforms of the Class DE rectifier are time reversed versions of the inverter waveforms. The underlying relationship connecting the two circuits is *time reversal duality* [14]. This concept can be touched upon only briefly in this paper.

The traditional duality between voltage and current has been well understood for many years. Time reversal duality is a different relationship, in which the corresponding waveforms of two systems are time reversed versions of each other. Time reversal in the context of dc-dc conversion has been demonstrated or remarked upon by several workers [11], [15–17]; however, they did not explore the relationship further. In fact it applies to a wide variety of physical systems.

Suppose  $D$  is an  $n$ -dimensional continuous dynamical system with state vector  $\mathbf{x} \in \mathbb{R}^n$ , characterised by the vector differential equation

$$\frac{d\mathbf{x}}{dt} = \mathbf{f}[\mathbf{x}, t] \quad (20)$$

Given an initial condition  $\mathbf{x}(0)$ , equation (20) may be integrated to generate a state-space trajectory  $\mathbf{x}(t)$ . Now let  $D^\#$  be another dynamical system with state vector  $\mathbf{x}^\# \in \mathbb{R}^n$ , such that

$$\frac{d\mathbf{x}^\#}{dt} = -\mathbf{f}[\mathbf{x}^\#, -t] \quad (21)$$

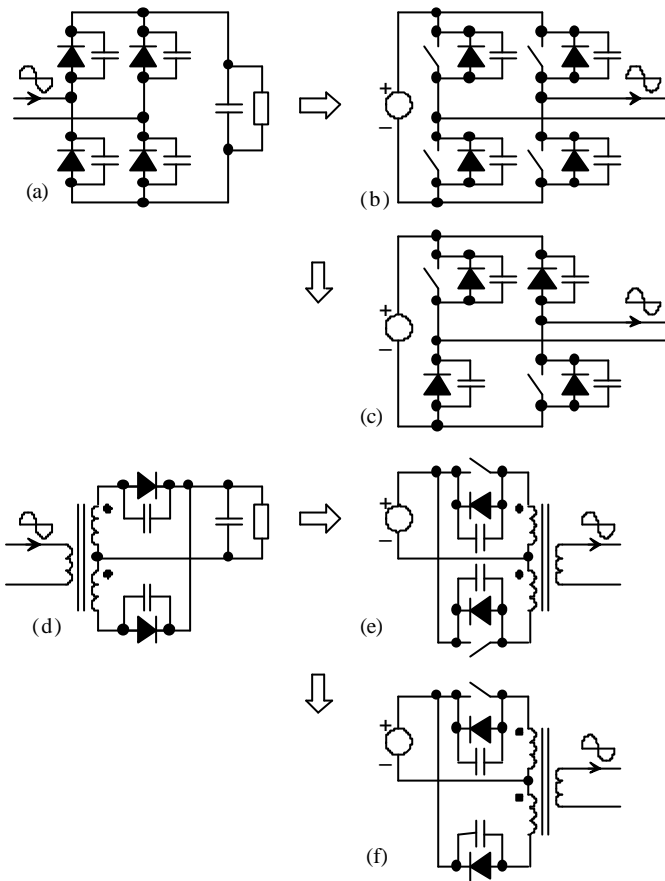
and  $\mathbf{x}^\#(0) = \mathbf{x}(0)$ . It can be shown that  $\mathbf{x}^\#(t) = \mathbf{x}(-t)$  for all  $t$ , i.e. the corresponding waveforms are time reversed versions of each other. The systems  $D$  and  $D^\#$  are time reversal duals.

This result can be applied to electrical networks. It turns out that there are four ways to form the time reversal dual of a circuit. Of these, the most intuitive and useful is Type 1 duality, in which the reference direction of all currents is inverted. Suppose an animated film were to show the operation of a circuit with its currents represented by moving charges. Projected in reverse, the charges would move backwards, while the voltages would remain in their original polarity. All waveforms would be time reversed. Because current is negated but not voltage, power in the time reversal dual circuit is also negated: the direction of energy flow is reversed. This allows a rectifier to be turned into an inverter, for example.

To proceed further, the theory must be extended to include switches and diodes. Certain difficulties arise with switches, but work is under way to clarify them. A time reversed ideal diode may always be replaced by an appropriately driven ideal switch.

### VII. OTHER CLASS DE CONVERTER TOPOLOGIES

Time reversal duality forms the basis for transforming Class DE rectifiers into the corresponding inverters. The Class DE rectifier of Fig. 6 can be derived from a simple half wave



converters operating in the megahertz frequency range. These should offer high efficiency, good electromagnetic compatibility and the potential for miniaturisation.

Fig. 10: Class DE rectifier–inverter pairs. The full bridge rectifier (a) transforms under time reversal duality to the full bridge inverter (b), or its degenerate form (c), the asymmetric half bridge inverter. The full wave rectifier (d) transforms to the push-pull inverter (e), or its degenerate form (f), the forward converter. (Matching networks are not shown.)

doubler type rectifier by adding shunt capacitance to the diodes. Time reversal duality allows the synthesis of the corresponding inverter, the half bridge inverter of Fig. 2. It is not difficult to apply the same principle to other rectifiers and so devise other Class DE ZVS inverters. Examples are shown in Fig. 10. Bidirectional converters are also possible. Furthermore, voltage–current duality can be applied independently, generating *dual Class DE* converters with ZCS. These may be useful with devices such as IGBTs, or when stray inductance is problematical.

### VIII CONCLUSION

This paper has described a Class DE inverter and rectifier, whose smooth switching transitions make them suited to high frequency dc-dc conversion. The rectifier and inverter are linked by a time reversal duality relationship. Applying this to other rectifier circuits permits the synthesis of further members of the Class DE family. With appropriate matching and control circuits, it is hoped that they will lead to Class (DE)<sup>2</sup> dc-dc

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