CHAOTIC BEHAVIOUR IN CURRENT-MODE CONTROLLED DC–DC CONVERTOR

Indexing terms: Convertors, Stability, Chaos

An approximate mapping is derived for a current-mode controlled buck convertor, leading to a stability criterion. Conditions are derived under which chaos in a strict sense occurs, and bounds on the inductor current are found.

Introduction: It is well known that many current-mode controlled DC–DC convertors are prone to instability,[1,2] the usual criterion being that the switch duty factor exceeds 50%. It is shown, in a particular case, that what has up to now been referred to as instability is in fact chaos.

Current-mode controlled buck convertor: Consider the circuit of Fig. 1 and the waveforms of Fig. 2. The circuit is employed to convert an input voltage V_I into an output voltage $v \simeq V_{ref}$. Switch S is controlled by an R-S latch that is set by clock pulses of period T; with the latch set, S is closed. The current i in L is converted by transresistance R_s (a current-sensing amplifier) into a sawtooth voltage $i(t)R_s$. The error signal $v_e(t) = V_{ref} - v$ is amplified with gain A. A comparator produces a pulse if $iR_s \geq Av_e$, resetting the latch and opening S. (Reset dominates over set.) In the periodic state all waveforms have period T, but under certain conditions subharmonics and chaos can occur, e.g. if $iR_s < Av_e$ for longer than a single clock cycle.

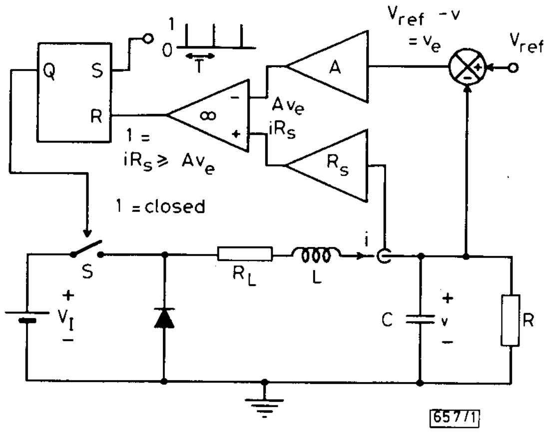

Fig. 1 *Circuit diagram of current-mode controlled buck convertor*

In the following analysis, operation of the buck convertor is confined to the continuous conduction mode, i.e. $i > 0$ at all times.

Mapping: A mapping F describes the behaviour of the inductor current by relating the current i_{n+1} as S closes to the current i_n at the previous closing of S; i.e. $i_{n+1} = F(i_n)$, $n = 0, 1, 2, \ldots$.

The mapping is now derived with the following assumptions:

(1) capacitor C is large enough that the ripple in the load voltage v can be neglected ($RC \gg T$)

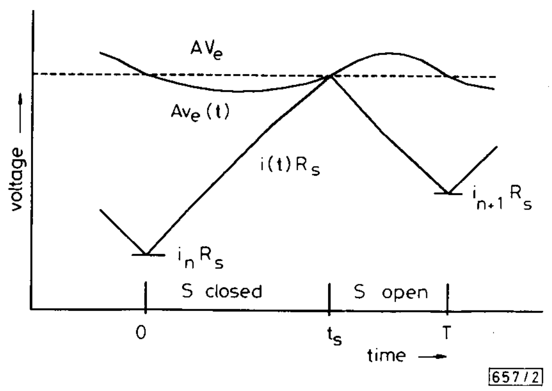

Fig. 2 *Waveforms appearing in circuit of Fig. 1*

(2) the quantity $R_f \triangleq R_s/A$ is small, i.e. the loop gain is large ($R \gg R_f$)

(3) the diode and switch are ideal; the inductor is allowed to have a small series resistance R_L ($L/R_L \gg T$).

Assumption 1 means that the error voltage $v_e(t)$ is essentially constant. An expression for this constant, V_e, is now found. The average power supplied by V_I is equal to the average power dissipated in R_L plus that dissipated in R, namely $(V_{ref} - V_e)^2/R$. This leads to an equation which can be solved approximately for V_e, where the approximation involves a first-order Taylor expansion in the small quantities V_e/V_{ref} and $R_L T/L$. The symbolic manipulation program Macsyma gives

$$V_e \simeq V_{ref} \frac{R_f}{R} \left[\frac{T(R_L + R)^2(1 - V_{ref}/V_I) + 2LR}{2L(2R_f + R_L + R)} \right] \tag{1}$$

The inductor current increases from $t = 0$ (when S last closed) until $iR_f = V_e$. This occurs at t_s, when S opens. The latch ensures that S remains open until the next clock pulse.

Assumption 1 implies that i follows an exponential charging or discharging curve, depending on the state of S. Assumption 3 allows the curve to be linearised as

$$i(t) \simeq \begin{cases} i_n + (V_I - V_{ref} - i_n R_L)t/L & (2a) \\ \quad 0 \le t < t_s & \\ V_e/R_f - (V_{ref} + V_e R_L/R_f)(t - t_s)/L & (2b) \\ \quad t_s \le t < T & \end{cases}$$

Because $i(t_s) = V_e/R_f$, t_s can be found from eqn. 2a as

$$t_s = \frac{L(V_e - R_f i_n)}{R_f(V_I - V_{ref} - i_n R_L)} \tag{3}$$

Substituting this into eqn. 2b gives

$$i_{n+1} = \frac{V_e}{R_f} - \frac{T(V_{ref} R_f + V_e R_L)}{LR_f} \left[1 - \left(\frac{t_s}{T} \right) \text{mod } 1 \right] \tag{4}$$

(The quantity t_s/T is expressed modulo 1 to allow for the fact that clock pulses have no effect if they arrive while S is closed.) The mapping F is found by substituting t_s into eqn. 4.

Onset of instability: A value i^* such that $i^* = F(i^*)$ is a fixed point of the mapping. If $|F'(i^*)| < 1$, the fixed point is stable and $i(t)$ is periodic with period T. If not, subharmonics or chaos may occur.

If $i(t)$ is of period T, the duty factor is given by

$$\frac{t_s}{T} = \frac{V_{ref} - V_e}{V_I} \left(1 + \frac{R_L}{R} \right) \tag{5}$$

(If not, this result still holds, but the duty factor is now an average over many cycles.) This steady-state value of t_s can be used in eqn. 3 to solve for i^*. The mapping can be differentiated with respect to i_n, and i^* substituted for i_n, to find the value of V_I at which $|F'(i^*)| = 1$. This V_I indicates where period T behaviour first becomes unstable, undergoing a bifurcation to period $2T$ or to chaos. It is given approximately by

$$V_{I[bif]} \simeq 2V_{ref} + V_{ref} \frac{R_L}{R} \times \left[\frac{4LR - T(R_L + R)(4R_f + R_L + R)}{2L(2R_f + R_L + R)} \right] \tag{6}$$

where assumptions 1–3 have been used to simplify the expression. If $R_L = 0$ then $V_{I[bif]} = 2V_{ref}$, implying that the duty factor of S is 50%, as derived in Reference 1.

Chaos: The mapping, eqns. 3 and 4, can be put in the form $i_{n+1} = 1 - [\alpha(i_n) + \beta]$ mod 1, which has been proved[3] to produce a strictly chaotic sequence if the function $\alpha(\ )$ is non-negative and Lipschitz, with Lipschitz constant strictly greater than unity. Because our $\alpha(\ )$ is continuous, the inductor current will be strictly chaotic when $|\alpha'(i_n)| > 1$ for all i_n, i.e.

$$V_{ref} < V_I < 2\left(V_{ref} + \frac{V_e R_L}{R_f} \right) \tag{7}$$

The sequence $\{i_n\}$ is bounded; eqn. 4 shows that the upper bound on i is reached when $t_s = T$ and the lower bound when $t_s = 0$. The limits on the inductor current are thus

$$\frac{V_e}{R_f} - \frac{TV_{ref}}{L} \le i \le \frac{V_e}{R_f} \tag{8}$$

where assumption 3 has been used to simplify the left-hand side.

Conclusion: We have analysed a simple model of an unstable, uncompensated current-mode controlled convertor to establish that, subject to the approximations made in the analysis, its operation is strictly chaotic. The importance of establishing chaos is that chaotic waveforms, although noiselike, are bounded; therefore the circuit can be engineered to operate reliably in a chaotic mode. One benefit might be improved transient response, because the design is no longer constrained by stability considerations.

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